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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,383	02/06/2004	Salman Akram	MI22-2469	6354

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EXAMINER	
ABRAHAM, FETSUM	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,383	AKRAM ET AL.	
	Examiner	Art Unit	
	Fetsum Abraham	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/9/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-43 and 53-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *the rest* is/are rejected.

7)☒ Claim(s) *34-36,58,59,65,66 and 74* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 32,33,37-43,53-57,60,62-64,67-72,75-83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunga et al (5,5,22,215) in view of Radosevich et al (6,865,080).

As for claims 32,42,43,53-55,57,62-64,67,68 the primary reference teaches the following;

Detailed Description Text (6):
The heat conduction plate 11 has a wafer temperature sensor 17 mounted in a central region thereof for measuring the temperature Tw of the wafer W.

Here, the prior art asserts the fact that wafers were sensed for temperature in wafer processing procedures.

Further, the prior art asserts that interconnect wiring were associated with the signal processing aspect of the wafer temperature sensing process as such:

Detailed Description Text (7):
Referring to the block diagram shown in FIG. 3, the wafer temperature sensor 17 and plate temperature sensor 19 are connected to a microcomputer 22, along with a first temperature setter 20 for setting the wafer cooling target temperature Tsw (e.g. 20.degree. C.) and a second temperature setter 21 for setting an initial temperature Tsp of the cooling plate assembly 5. Further, a controller 23 for controlling the air cylinder 10 and a driver 24 for driving the Peltier elements 15

are connected to the microcomputer 22.

In the following texts, the process involves indirect feedback control to normalize wafer temperature upon comparison to a reference temperature.

Detailed Description Text (9):
The wafer detector 25 compares the temperature measured by the wafer temperature sensor 17 and a predetermined temperature (e.g. 50.degree. C.) higher than the wafer cooling target temperature Tsw. Thus, the detector 25 detects the wafer W placed on the cooling plate assembly 5, based on an incoming wafer temperature Tw.sub.0 which is a high temperature prior to cooling, and outputs a cooling start signal.

Detailed Description Text (11):
The control device 27 compares the temperature Tw of wafer W detected by the wafer temperature sensor 17 and the target temperature Tsw set through the first temperature setter 20. When the temperature Tw equals the target temperature Tsw, the control device 27 outputs a cooling finish signal to the controller 23. Then, the substrate support pins 7 are raised to move the wafer W to a position spaced from and outside the sphere of thermal influence of the cooling plate assembly 5.

The primary reference discloses all the method procedures of the claimed invention but may not have been detailed so far as the sensor positioned over the wafer. However, the secondary reference shows a structure in figure 18 whereby a substrate supporting electronic circuits (184) is positioned on plate (148) and a temperature sensor (188) positioned over the circuits and bonded to the same through bonding layers(186). Therefore, it would have been obvious to one skilled in the art to use the topology of the secondary reference in the

primary refernce, since positioning a wafer temperature sensor on a the wafer saves space by allowing the wafer to be the subject of testing and the sensor support system simultaneously.

So far as claims 33,56 are concerned, interconnecting such devices is flexible to allow various interconnect types in the art. Signal processing between the computer and the circuits is formed by wire interconnect means that categorically include wire bonding.

As for claim 37, the temperature sensors in the prior arts are formed elements.

As for claims 38,60 for a sensor to sense temperature, it will have to resist the temperature. Temperature changes the characteristics of electronic elements and the change is resisted in terms of sensing the same. A temperature sensor is also a transducer when the sensation results in electrical output. This means that the sensor is capable of producing electrical results upon sensing temperature. And any element capable of producing electrical signals upon an input comprises resistance by default and can be classified as a resistor from broader aspect of definition. Therefore, the sensors in the prior arts are resistors in that context.

As for claims 39,68 the prior arts have external interconnect means that connects them to external circuits.

As for claims 40,69 the connection of the sensor in the primary art with the wafer could be anywhere in the wafer since the wafer is uniformly doped and has continuous resistance implying that any point on it represents the electrical characteristics of all points on it.

As for claim 41,70 conductive traces are one of the most known conductive paths in the art and especially when they are applied to wafers. Semiconductor elements are formed on semiconductor wafers and traces are the

most practical means of interconnections between devices in the chip because they do not require large area as would be in the case of bumps and pads. They are also better efficient than wires in terms of reliability because they are integral parts of the wafer.

As for claim 71, the wafer and sensing structures are formed by exposure to manufacturing conditions and the wafer serves as the base element for making electronic circuits.

As for claim 72 see the Detailed Description Text (7) above. The prior art at least adjusts wafer cooling temperature upon sensing its temperature.

As for claim 75 the wafer in the primary reference is used to form electronic circuits.

As for claim 76,78,80,82, a semiconductor wafer in general or as a domain encapsulates silicon, which is the most common and basic material known in the art.

As for claims 77,79,81,83 there is no restriction in the primary art as to when the process of measuring wafer temperature takes place. Therefore, it indirectly includes at any stage of the wafer.

Claims 61,73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunga et al (5,5,22,215) in view of Radosevich et al (6,865,080) and further in view of Van Bilsen et al (6,121,061).

The first two prior arts disclose all subject matter claimed but multiple sensors sensing the temperature uniformity of a wafer. However, the third prior art teaches the missing link as such:

Detailed Description Text (9):
A plurality of temperature sensors are positioned in proximity to the wafer 16. The temperature sensors may take any of a variety of forms, such as optical pyrometers or thermocouples. The number and positions of the temperature sensors are selected to promote temperature uniformity, as will be understood in light of the description below of the preferred temperature controller. Preferably, however, the temperature sensors directly or indirectly sense the temperature of a position in proximity to the wafer.

CLAIMS:

17. The method of claim 11, further comprising controlling the temperature of a plurality of temperature sensors distributed in proximity to the wafer to maintain a uniform temperature distribution across the wafer at the steady state temperature.

Therefore, it would have been obvious to one skilled in the art to use multiple sensors to evaluate the uniformity of wafer temperature all over the wafer since the practice can provide assurance to circuit uniformity that may be formed on the substrate.

Claims 34-36,58,59,65,66,74 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See US 6476886 B2:

TITLE: Method for assembling a tiled, flat-panel microdisplay array

Detailed Description Text (28):

Temperature sensor and heating devices can be designed and fabricated into the silicon tile back planes during the wafer fabrication process. For example, native electronic devices, such as semiconductor junction diodes and resistors, can be used for temperature sensing and tile heating purposes, respectively.

Electrical access to these devices and their control can, for example, be achieved via on-chip multi-layer metal interconnect and chip-to-package and package-to-flex connections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham

3/28/06